FAIRCHILD SEMICONDUCTOR®

May 2010

FDMA1024NZ

Dual N-Channel PowerTrench® MOSFET

20 V, 5.0 A, 54 mΩ

Features

- Max $r_{DS(on)}$ = 54 mΩ at V_{GS} = 4.5 V, I_D = 5.0 A
- Max $r_{DS(on)}$ = 66 mΩ at V_{GS} = 2.5 V, I_D = 4.2 A
- Max $r_{DS(on)}$ = 82 mΩ at V_{GS} = 1.8 V, I_D = 2.3 A
- Max $r_{DS(on)}$ = 114 mΩ at V_{GS} = 1.5 V, I_D = 2.0 A
- HBM ESD protection level = 1.6 kV (Note 3)
- Low profile - 0.8 mm maximum - in the new package MicroFET 2x2 mm
- RoHS Compliant
- Free from halogenated compounds and antimony oxides

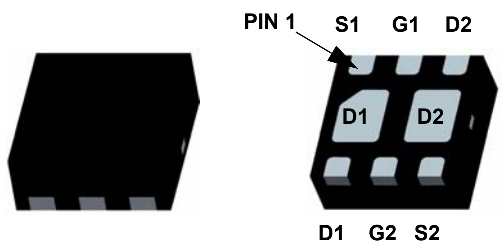
General Description

This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses.

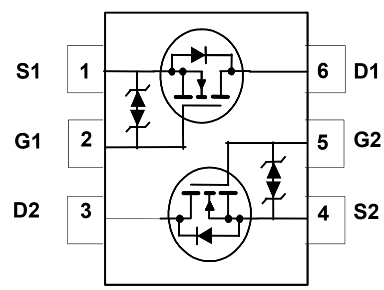
The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Applications

- Baseband Switch
- Loadswitch
- DC-DC Conversion



MicroFET 2x2



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		20	V
V_{GS}	Gate to Source Voltage		±8	V
I_D	Drain Current -Continuous	(Note 1a)	5.0	A
	-Pulsed		6.0	
P_D	Power Dissipation	(Note 1a)	1.4	W
	Power Dissipation	(Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	86 (Single Operation)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	173 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	69 (Dual Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	151 (Dual Operation)	

Package Marking and Ordering Information

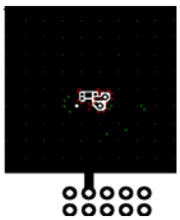
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
024	FDMA1024NZ	MicroFET 2X2	7 ”	8 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

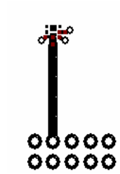
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		19		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, I_D = 250 μA	0.4	0.7	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-3		mV/°C
$r_{DS(on)}$	Static Drain to Source On-Resistance	V_{GS} = 4.5 V, I_D = 5.0 A		37	54	mΩ
		V_{GS} = 2.5 V, I_D = 4.2 A		43	66	
		V_{GS} = 1.8 V, I_D = 2.3 A		52	82	
		V_{GS} = 1.5 V, I_D = 2.0 A		67	114	
		V_{GS} = 4.5 V, I_D = 5.0 A, T_J = 125 °C		51	75	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 5.0 A		16		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz		375	500	pF
C_{oss}	Output Capacitance			70	95	pF
C_{rss}	Reverse Transfer Capacitance			40	65	pF
R_G	Gate Resistance	f = 1 MHz		4.3		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10 V, I_D = 5.0 A V_{GS} = 4.5 V, R_{GEN} = 6 Ω		5.3	11	ns
t_r	Rise Time			2.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			18	33	ns
t_f	Fall Time			2.3	10	ns
Q_g	Total Gate Charge	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 5.0 A		5.2	7.3	nC
Q_{gs}	Gate to Source Gate Charge			0.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			0.9		nC
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Source-Drain Diode Forward Current				1.1	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.1 A (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 5.0 A, di/dt = 100 A/μs		19	35	ns
Q_{rr}	Reverse Recovery Charge			5	10	nC

Notes:

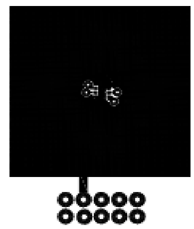
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
   (a) $R_{\theta JA}$ = 86 °C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.
   (b) $R_{\theta JA}$ = 173 °C/W when mounted on a minimum pad of 2 oz copper. For single operation.
   (c) $R_{\theta JA}$ = 69 ^{o}C/W when mounted on a 1 in^2 pad of 2 oz copper, 1.5 ” x 1.5 ” x 0.062 ” thick PCB. For dual operation.
   (d) $R_{\theta JA}$ = 151 ^{o}C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



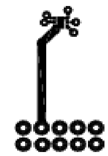
a) 86 ^{o}C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 173 ^{o}C/W when mounted on a minimum pad of 2 oz copper.



c) 69 ^{o}C/W when mounted on a 1 in^2 pad of 2 oz copper.



d) 151 ^{o}C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0 %
3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

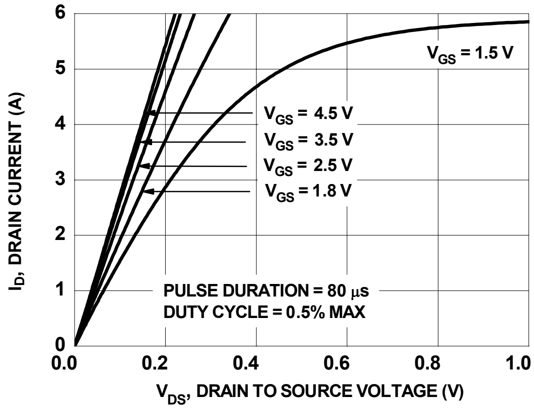


Figure 1. On-Region Characteristics

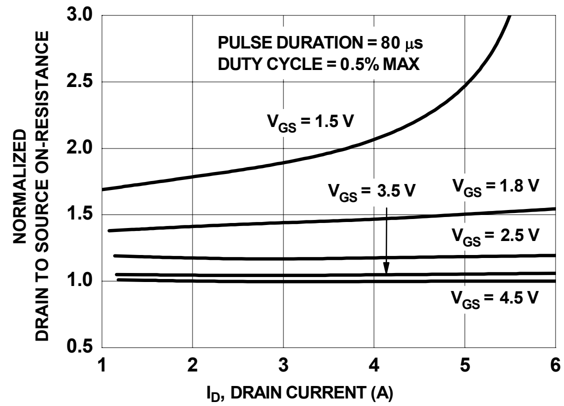


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

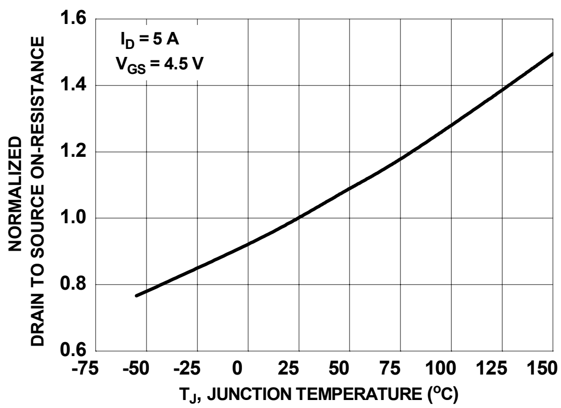


Figure 3. Normalized On-Resistance vs Junction Temperature

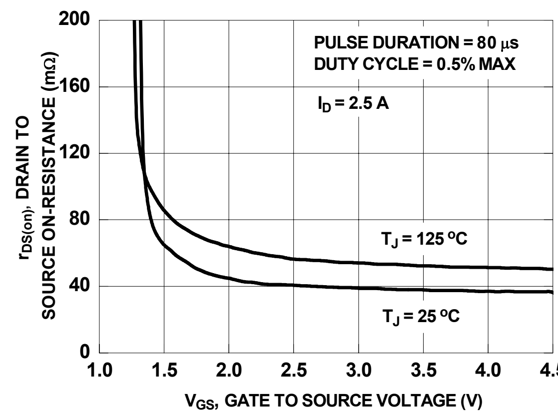


Figure 4. On-Resistance vs Gate to Source Voltage

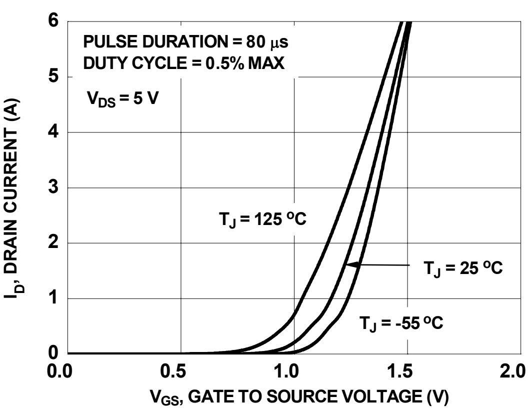


Figure 5. Transfer Characteristics

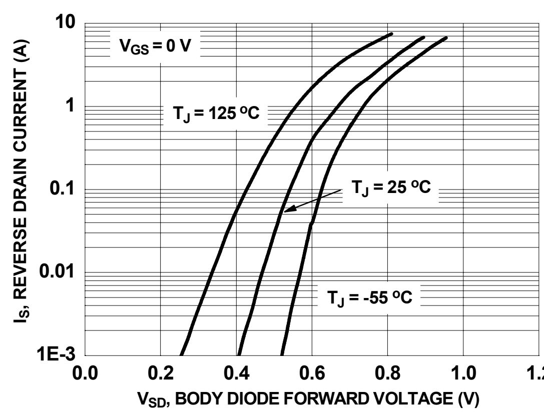


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

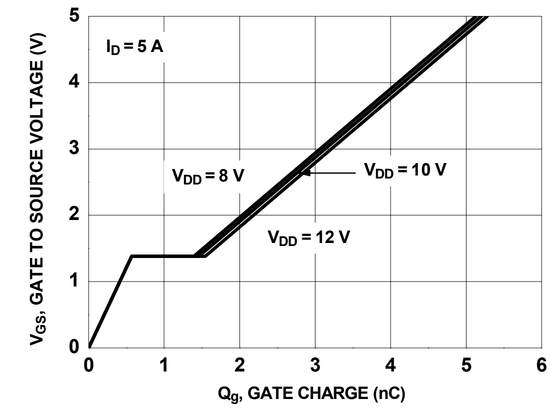


Figure 7. Gate Charge Characteristics

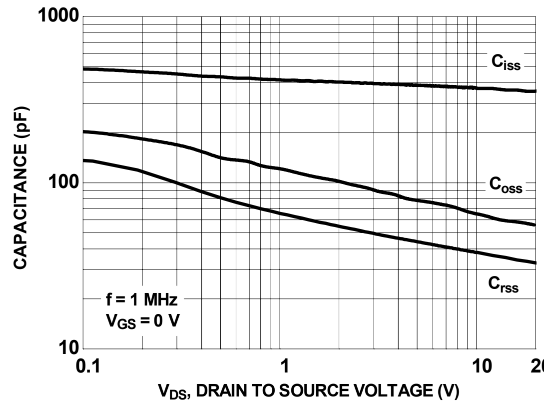


Figure 8.Capacitance vs Drain to Source Voltage

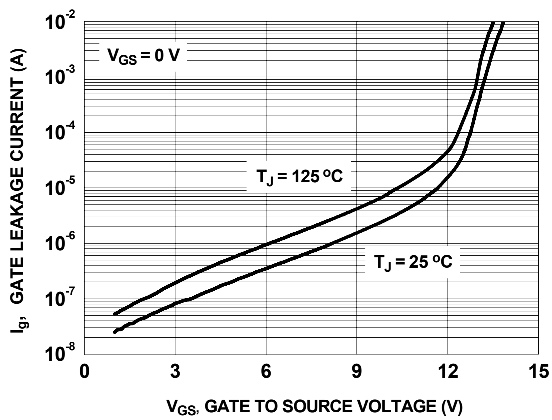


Figure 9. Gate Leakage Current vs Gate to Source Voltage

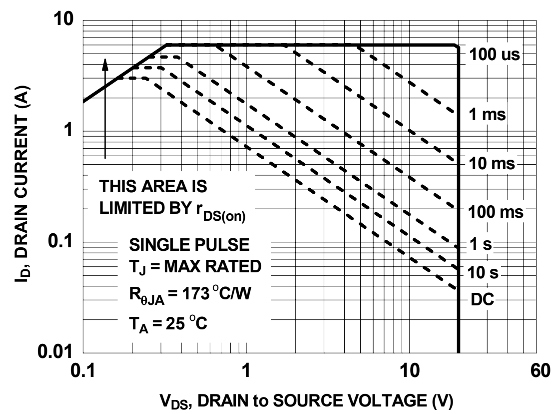


Figure 10. Forward Bias Safe Operating Area

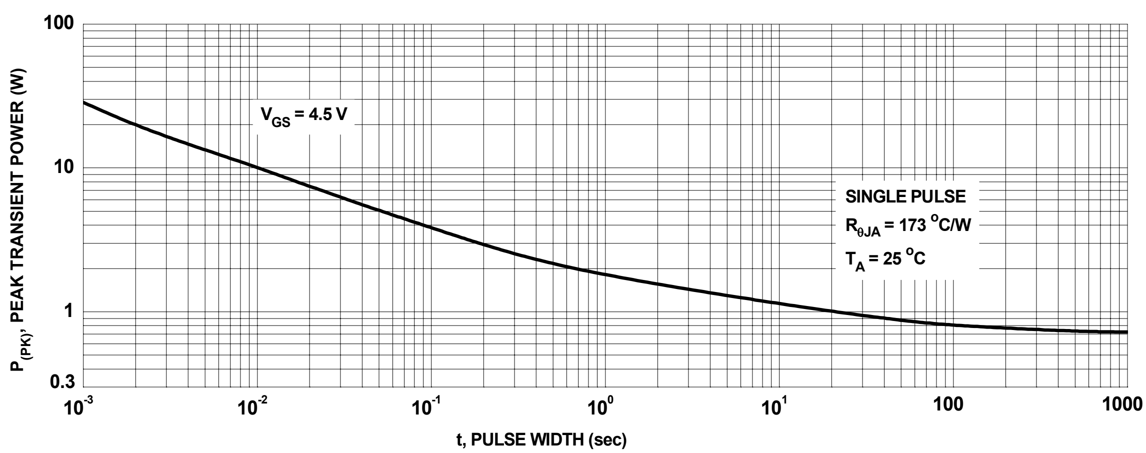


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

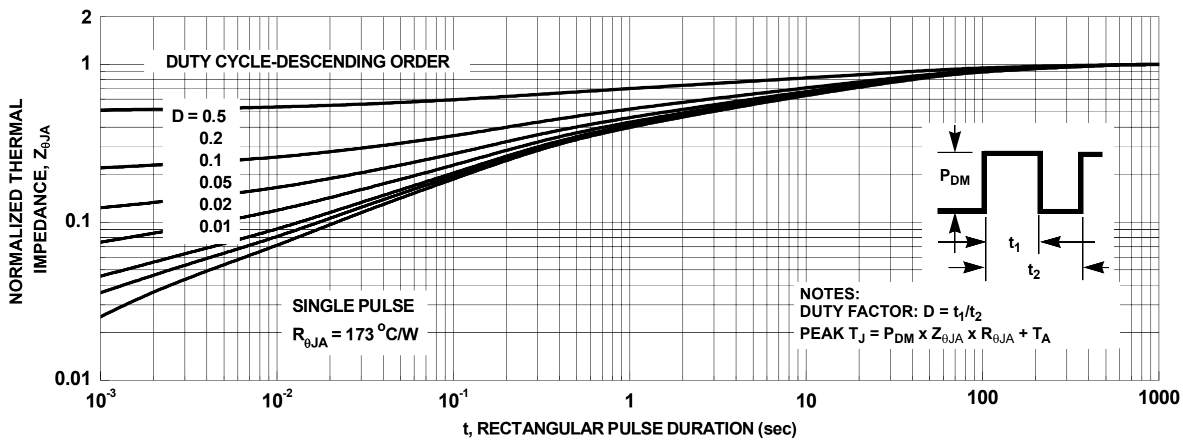
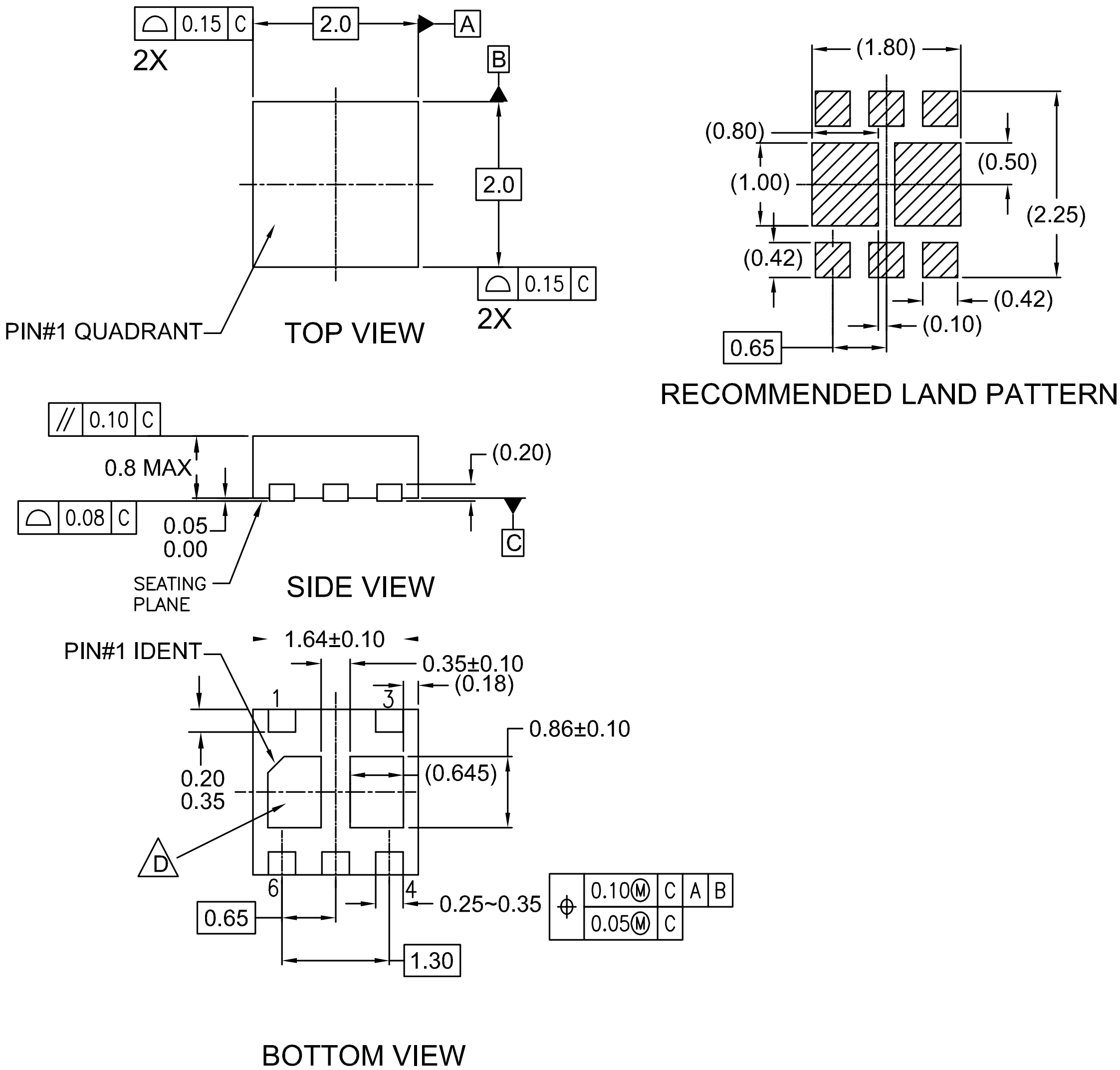


Figure 12. Junction to Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC EXCEPT AS NOTED.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. NON-JEDEC DUAL DAP

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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